1. A method of forming an opening in a stack of insulator layers, comprising the steps of:

providing a conductive structure;

forming said stack of insulator layer on said conductive structure, with said stack of insulator layers comprised of an a first liner layer, an overlying first insulator layer, a second liner layer, an overlying second insulator layer, an anti-reflective coating (ARC), layer; and a capping, third insulator layer;

forming a via opening in a first portion of said stack of insulator layer, with said via opening terminating in said first liner layer;

forming a trench opening in a second portion of said stack of insulator layers using a photoresist shape as an etch mask, with said trench opening terminating on top surface of said second liner layer, and forming a photoresist plug in said via hole, located on said first liner layer;

removing portion of said second liner layer exposed in said trench opening;

removing said photoresist shape and said photoresist plug; and

removing portion of said first liner layer exposed in said via opening, exposing a portion of a top surface of said conductive structure.

2. The method of claim 1, wherein said conductive structure is comprise of copper.

3. The method of claim 1, wherein said first liner layer is a silicon nitride layer, obtained via plasma enhanced chemical vapor deposition (PECVD) procedures at a thickness between about 400 to 600 Angstroms.

4. The method of claim 1, wherein said first insulator layer is a fluorinated silica glass (FSG) layer, obtained via PECVD procedures at a thickness between about 500 to 1000 Angstroms.

5. The method of claim 1, wherein said second liner layer is a silicon nitride layer, obtained via PECVD procedures at a thickness between about 200 to 400 Angstroms.

6. The method of claim 1, wherein said second insulator layer is a silicon oxide layer, obtained via PECVD procedures at a thickness between about 500 to 1000 Angstroms.

7. The method of claim 1, wherein said ARC layer is a silicon oxynitride layer, obtained via PRCVD procedures to a thickness between about 500 to 700 Angstroms.

8. The method of claim 1, wherein said capping, third insulator layer is a silicon oxide layer, obtained via PECVD procedures at a thickness between about 500 to 700 Angstroms.

9. The method of claim 1, wherein said via opening is defined in said capping, third insulator layer, in said ARC layer, in said second insulator layer, in said second liner layer, and in said first insulator layer, via an anisotropic reactive ion etching (RIE) procedure, using CHF_3 as an etchant for said capping, third insulator layer, for said second insulator layer, for said ARC layer and for said first insulator layer, while CH_xF_y or CF_4 is used as an etchant for said second liner layer.

10. The method of claim 1, wherein the diameter of said via opening is between about 0.25 to 2.5 um.

11. The method of claim 1, wherein said trench opening is defined in said capping, third insulator layer, in said ARC layer, and in said second insulator layer via an anisotropic RIE procedure using CHF_3 as an etchant.

12. The method of claim 1, wherein portion of said second liner layer exposed in said trench opening, is removed via a selective RIE procedure using CF_4 or CH_xF_y as an etchant.

13. The method of claim 1, wherein said photoresist shape and said photoresist plug are removed using plasma oxygen ashing procedures.

14. The method of claim 1, wherein portion of said first liner layer exposed in said via opening, is removed via a selective RIE procedure using CF_4 or CH_xF_y as an etchant.

15. The method of claim 1, wherein the etch rate ratio of silicon nitride of said first liner layer, to silicon oxide, during the selective RIE procedure used to remove portion of said first liner layer exposed in said via opening, is between about 5 to 1, to 10 to 1 using CF_4 or CH_xF_y as an etchant.

16. A method of forming a dual damascene opening in a stack of insulator layers featuring a two step stop layer removal procedure, comprising the steps of:

providing a copper structure;

forming said stack of insulator layers on said copper structure, with said stack of insulator layers comprised of an underlying first silicon nitride stop layer, an overlying first dielectric layer, a second silicon nitride stop layer, a second dielectric layer, an anti-reflective coating (ARC) layer, and a capping silicon oxide layer;

forming a via opening in a first portion of said stack of insulator layer, with said via opening terminating in said first silicon nitride stop layer;

forming a trench opening in a second portion of said stack of insulator layers using a photoresist shape as an etch mask, with said trench opening terminating on top surface of said second silicon nitride stop layer, and forming a photoresist plug in said via hole, overlying a portion of top surface of said first silicon nitride stop layer;

performing a first step of said two step stop layer removal procedure to selectively remove portion of said second silicon nitride stop layer exposed in said trench opening;

removing said photoresist shape and said photoresist plug; and

performing a second step of said two step stop layer removal procedure to remove portion of said first silicon nitride stop layer exposed in said via opening, exposing a portion of a top surface of said copper structure.

17. The method of claim 16, wherein said first silicon nitride stop layer is obtained via plasma enhanced chemical vapor deposition (PECVD) procedures at a thickness between about 400 to 600 Angstroms.

18. The method of claim 16, wherein said first dielectric layer is an FSG layer, obtained via PECVD procedures at a thickness between about 500 to 1000 Angstroms.

19. The method of claim 16, wherein said second silicon nitride stop layer is obtained via PECVD procedures at a thickness between about 200 to 400 Angstroms.

20. The method of claim 16, wherein said second dielectric layer is a silicon oxide layer, obtained via PECVD procedures at a thickness between about 500 to 1000 Angstroms.

21. The method of claim 16, wherein said ARC layer is a silicon oxynitride layer, obtained via PECVD procedures to a thickness between about 500 to 700 Angstroms.

22. The method of claim 16, wherein said capping, silicon oxide layer is obtained via PECVD procedures at a thickness between about 500 to 700 Angstroms.

23. The method of claim 16, wherein said via opening is defined in said capping silicon oxide layer, in said ARC layer, in said second dielectric layer, in said second silicon nitride stop layer, and in said first dielectric layer via an anisotropic reactive ion etching (RIE) procedure, using CHF_3 as an etchant for said capping silicon oxide layer, for said ARC layer and for said second dielectric layer and for said first dielectric layer, while CF_4 or CH_xF_y is used as an etchant for said second silicon nitride stop layer.

24. The method of claim 16, wherein the diameter of said via opening is between about 0.25 to 2.5 um.

25. The method of claim 16, wherein said trench opening is defined in said capping silicon oxide layer, in said ARC layer, and in said second dielectric layer, via an anisotropic RIE procedure using CHF_3 as an etchant.

26. The method of claim 16, wherein said first step of said two step stop layer removal procedure, used to selectively remove portion of said second silicon nitride stop layer exposed in said trench opening, is performed via a selective RIE procedure using CF_4 or CH_xF_y as an etchant.

27. The method of claim 16, wherein said photoresist shape and said photoresist plug are removed using plasma oxygen ashing procedures.

28. The method of claim 16, wherein said second step of said two step stop layer removal procedure, used to selectively remove portion of said first silicon nitride stop layer exposed in said via opening, is performed via a selective RIE procedure using CF_4 or CH_xF_y as an etchant.

29. The method of claim 16, wherein the etch rate ratio of silicon nitride to silicon oxide, during said second step of said two step stop layer removal procedure performed via a selective the selective RIE procedure used to remove portion of said first silicon nitride stop layer exposed in said via opening, is between about 5 to 1, to 10 to 1 using CF_4 or CH_xF_y as an etchant.